ABSTRACT

Methods and apparatus for handling speculative addresses in a pipelined digital processor are provided. A digital signal processor includes an address generator configured to generate speculative data addresses, a pipelined execution unit configured to execute instructions using data at locations specified by the speculative data addresses, a speculative register file configured to hold the speculative data addresses as corresponding instructions advance through the execution unit, an architectural register file configured to hold architectural data addresses, and control logic configured to write speculative data addresses to the speculative register file as the speculative data addresses are generated by the address generator and to supply speculative data addresses or architectural data addresses to the address generator. The speculative register file may be configured with sufficient capacity to hold one or more architectural data addresses.